## REMARKS/ARGUMENTS

Examiner Tran is thanked for his thorough examination of the subject Patent Application. The Examiner is also thanked for indicating Claims 10-32 are allowable over the prior art of record. The Claims have been have been carefully reviewed, several Claims have been amended in response to the Examiner's kind comments, and all Claims are now considered to be in condition for Allowance.

An "and" was inserted where appropriate in all claims 1-32.

Reconsideration of the objection to Claims 2 through 9 is requested, in light of the following.

Claim 1 upon which claims 2 through 9 are dependent is a valid claim not anticipated by Yamazaki et al. as discussed below.

Reconsideration of the rejection of Claim 1 under 35 U.S.B. 102(e) as being anticipated by Yamazaki et al. (U.S. Patent No. 5,434,562), is requested, in light of the following.

The claimed invention relates to verification of sense and program operations for a non-volatile memory, and Claim 1 claims the circuit elements of the non-volatile memory related to program verify. Yamazaki et al. relates to a multi power semiconductor integrated circuit device containing a plurality of supply voltages, and

more specifically, Yamazaki et al. relates to the power supply structure of a system LSI in which logic such as a processor and a DRAM (dynamic random access memory) are integrated on the same semiconductor chip (col. 1, lines 11-15). The objective of Yamazaki et al. is to provide a semiconductor integrated circuit device having a multi power structure with a reduced power consumption including a first power-on detection circuit responsive to a first power supply voltage for detecting application of the first power supply voltage to activate a first power-on detection signal according to the detection results, a second power-on detection circuit responsive to a second power supply voltage for detecting application of the second power supply voltage to activate a second power-on detection signal according to the detection results, and a main power-on detection circuit coupled to the first and second power-on detection circuits for generating a main power-on detection signal that is activated while at least one of the first and second power-on detection signals is at an active state (col. 3, lines61-67), (col. 4, lines 1-11) and (col. 4-26, lines1-67).

With respect to claim 1, Yamazaki et al. does not disclose, as the Examiner suggests, a program verify circuit for non-volatile memory cells, comprising: a) a non-volatile memory chip [MA], b) a bit line read path [within MA], c) a reference read path [within MA], d) a voltage control circuit [CTL] connected in said read path and said reference path, e) a sense amplifier [SA], f) an equalizer circuit [2] to make voltages stored on the bit line read path and the reference read path a same amplitude [VDDL/VDDH having the same amplitude – see figure 4] and , g) an output node of the bit line read path and the output node of the reference read path connected to said

sense amplifier inputs [both are within MA]. In fact there is no description of [MA] by Yamazaki et al.

Relative to the above noted suggestion of the Examiner: The MA as disclosed by Yamazaki et al. is a DRAM and not a nonvolatile memory (col. 1, lines 11-15) and (col. 5, lines 43-67). The bit line read path and the reference read path and their operation are not discussed in Yamazaki et al., and furthermore, the reference read path is not a path required for a DRAM memory. The control circuit CTL in Yamazaki et al. is for controlling an operation for memory cell selection in the memory cell array MA (col.1, lines 59-61). The voltage control circuit in the claimed invention is used to precharge the bit line and the reference bit line during a read or verify operation (page 10, lines 9-12 of the claimed invention). VDDL in Yamazaki et al. is the logic power supply voltage (col. 6, lines 6-15) not the bit line read path voltage or the reference read path voltage as suggested by the Examiner. VDDH is the DRAM power supply voltage (col. 6, lines 21-23) and is neither the bit line read path voltage nor the reference read path voltage as suggested by the Examiner. The output node of the bit line read path and the output node of the reference read path connected to said sense amplifier inputs is not discussed, detailed or disclosed in Yamazaki et al., and it is presumptuous for the Examiner to assume the actual connection when (1) the connection is not discussed in Yamazaki et al. and (2) the memory array in Yamazaki et al. is a DRAM, not the non-volatile memory of the claimed invention.

Yamazaki et al. is an invention dealing with the powering a semiconductor chip, and the power on detection by the semiconductor chip. Yamazaki et al. does not disclose a program verify circuit for nonvolatile memory cells as stated in Claim 1 of the

claimed invention. The claimed invention and Yamazaki et al. are two completely different inventions, and the claimed invention is not anticipated by Yamazaki et al.

All Claims are now considered to be in condition for allowance.

Allowance of all Claims is Requested.

It is requested that should Examiner Tran not find that the Claims are now allowable, that he call the undersigned at (845) 452-5863 to overcome any problems preventing allowance.

Respectively submitted,

Stephen B. Ackerman,

Reg. No. 37,761